NTSC/PAL-M INPUT MODULE

Manual Number: A90-066337-01 TP No.: 06-056 Issue No.: 2

INTRODUCTION Refer to Figure 1. This module is used in both NTSC and PAL-M Systems.

The Input module equalizes the incoming video signal, controls the system video gain, and separates the chrominance, luminance, and sync signals. Specific functions performed by the Input module are listed below and discussed in the circuit description.

Common mode rejection of the input signal
Cable equalization
Video gain control
Chroma/luminance separation
Feedforward clamp
Feedback clamp
Sync separation
Generation of clamp pulses for the Output Module
Interface for remote control functions
Local controls
On-board power regulation for this module

CIRCUIT OVERVIEW (Refer to Figure 1)

The Input Amplifier operates as a common-mode, balanced, inverting video amplifier.

The Variable Cable Equalizer provides adjustable compensation for the dc and high-frequency losses of the input cable. Equalization is adjustable from zero (no equalization) to the maximum equalization provided by the equalizer submodule, which plugs into the Input Module.

The Variable Gain amplifier is virtually identical to the equalizing amplifier, and is used to control the overall gain of the signal. In addition to providing gain control, this amplifier also serves as a combining point for the feedforward correction signal from the clamp circuit.

The Chroma Separator is an active transversal filter consisting of two delay lines and two inverting buffer amplifiers. The buffer amplifiers are configured to compensate for the slight dc loss, and equalize the high frequency loss of the delay line. The outputs of the buffer amplifiers are combined with the output of the Variable Gain Amplifier through a resistor matrix to provide comb filter separation of high frequency (chroma) and low frequency (luminance) signals.

The video output of the equalizing amplifier is also applied to the clamping and sync separation circuitry. The Color Lock Module uses Separated Sync #1 as a timing signal. The second Separated Sync output is used by the Sync Generator Module for genlocking.

The Clamp circuit, driven by a third output of the Sync Separator, clamps at the tip of sync, supplying correction signals to the Input Amplifier and the Variable Gain Amplifier.

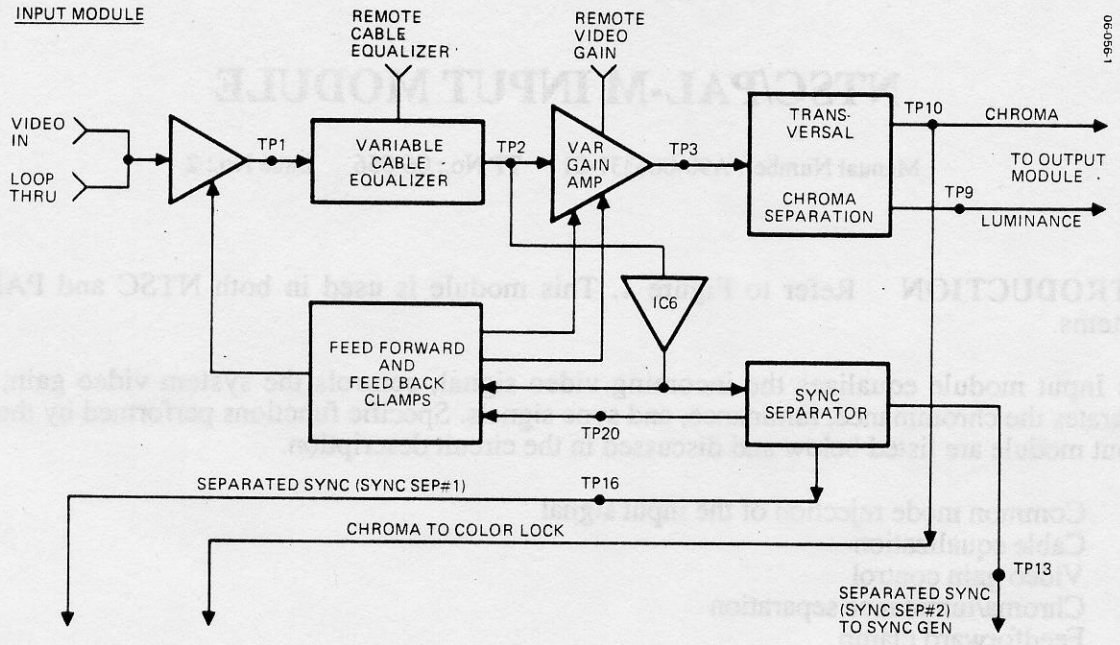


Figure 1. Input Module, Simplified Block Diagram

CIRCUIT DESCRIPTION Refer to schematic diagram E10-066337, and Figure 2.

Input Amplifier (sheet 1 of schematic, section D-E/5-8)

The input amplifier, which consists of Q1 through Q10 and associated components, operates as a common-mode, balanced, inverting video amplifier with an overall gain of approximately 0.65. Low frequency common mode rejection is performed by the balanced bridge circuits provided by RN1 and RN2. The high frequency common mode rejection may be trimmed with C4. The overall frequency response of the amplifier is controllable two ways: Capacitor C6 controls high frequency roll-off, and the combination of R16 and C7 controls mid-band roll-up to provide overall flat response through the video band.

In addition to the local video feedback through RN2-D and RN2-E, there is a low frequency feedback path from the video clamp circuit that goes through RN2-C to the base of Q2. This circuit path cancels low frequency hum at the input node of the amplifier, and thereby increases the overall dynamic range of the circuit.

Equalizing Amplifier (sheet 1 of schematic section D-E/2-4)

The equalizing amplifier, consisting of Q11 through Q19 and IC1 and associated components, is a feedback multiplier circuit with two paths from the input amplifier: one directly through R21 to one input node, and the other path through R22 (paralleled with an equalizer module assembly) to the other input node of the amplifier. The control voltage which comes from IC12 is fed to the upper port of the multiplier and determines whether the input signal through R21, or the input signal through R22 (in parallel with the equalizer module), or a linear combination of both of these signals is presented at the output. This, therefore, provides an equalizer circuit which can be adjusted from no equalization to the maximum equalization the equalizer board can provide.

Transistors Q11 and Q12 provide local feedback loops around the input transistors in IC1 to improve the overall linearity of the circuit. The signal then proceeds through the multiplier quad in IC1 and on to the Darlington gain amplifier stage, Q15 and Q16. Q18 and Q19 are biased by D6 and provide a complementary emitter follower output stage for added current gain in the amplifier. The signal then proceeds to the remote gain amplifier.

Remote Gain Amplifier (sheet 1 of schematic, B-C/6-8)

The remote gain amplifier is virtually identical to the equalizing amplifier. Since R45 and R46 have a 4:1 resistance ratio, the overall gain change of the amplifier is 4:1, or 12 dB. Its gain is nominally set at unity, so that it has a ± 6 dB gain control range. In addition to providing gain control, this amplifier is also used as a combining point for the feedforward signal from the clamp circuit. Since the amplifier has two nodes, and operates at two different gains, it is necessary to balance the clamp circuit at the maximum gain and minimum gain and provide two inputs to the remote gain amplifier. From the remote gain amplifier, the signal then proceeds to the chroma separator.

Chroma Separator (sheet 1 of schematic, A-C/3-5)

The chroma separator is an active transversal filter (i.e., one that combines a signal with its delayed and/or inverted counterpart) consisting of two delay lines and two inverting buffer amplifiers, which make up for the slight dc loss and equalize the high frequency loss of the delay line. The total delay of one section of the delay line and one of the amplifiers is equal to the period of one-half cycle of color subcarrier. The outputs of the amplifiers and the output of the remote gain amplifier are then combined through a resistor matrix to provide both high frequency signals and low frequency signals. This provides a phase linear (thus, no group delay) separation of chroma and luminance.

Resistor R183 allows the luminance component of the signal to be accurately nulled in the chroma combiner. From the chroma separator, the signals then proceed to the luminance and chroma amplifiers.

Luminance/Chroma Amplifiers (sheet 1 of schematic, A-C/1-2)

The luminance and chroma amplifiers buffer the two signals for distribution to other modules in the processor.

Sync Separator 1 (sheet 2 of schematic, sections A-B/2-8)

Introduction

Sync Separator 1 provides timing pulses for processor use only. It sends a short mid-sync pulse via TP20 to the clamp (IC8) and it coordinates the on/off times of Q69 and Q70 so the vertical interval's 9H sync pulses can be separated from the rest of the composite sync pulses (9H-) which come from Sync Separator 2 (Because of delays, these 9H and 9H- pulses are actually timed to occur at the back porch.). Finally it sends a sync pulse to the color lock board to generate the burst gate.

Description (Sync Separator 1)

The video signal from the output of the cable equalizing amplifier is also sent to clamping and sync separating circuitry of the Input module. The signal passes through R136 and DL1A, which is a four-pole transitional low-pass filter with a 2 MHz corner frequency. The signal is then amplified by IC6 and passed to several points within the clamping and sync separator circuitry. The path of first significance is through buffer (emitter follower) Q60 to the clamping diode formed by IC11C and the feedback transistor, Q59. This feedback pair functions as a clamp diode having an extremely square-cornered transfer characteristic at IC11 pin 7.

The initial rundown current for C65 is provided by R173 through the level shifter, IC11E, and current mirror, IC11A and IC11B. The signal which has been clamped is then buffered by Q61. The signal appearing at the emitter of Q61 is sync tip clamped with the sync tip referenced very nearly to ground. The actual dc value of sync tip is adjustable over a small range by R179 to accommodate offset errors in the sync separator, Q62 and Q63. At startup, the dc voltage on the base of Q63 is at ground, and R179 is set so that the negative tip of sync just turns on Q62. This produces a separated sync output at the collector of Q62 and Q64. R187 allows adjustment of the stored charge removal from Q64 and thereby provides a delay of the leading edge of sync. This is set for a 300 ns delay on start for the leading edge of sync.

From the collector of Q62, the separated sync signal follows two paths. The path of first significance is through R193 to buffer transistor Q65. Diodes D23 and D24, in conjunction with C79, R192, and the current pulses from Q65, provide a retriggerable monostable function that keeps D24 turned off unless the sync separator misses a sync pulse, in which case R192 will charge C79 high enough to turn on D24 and current will flow through R192 to pin 13 of IC11. This current is level shifted and mirrored back to the rundown circuit. This ensures that if a large negative noise spike has entered the processor and charged C65 to a voltage where sync is no longer crossing the threshold of Q62, a missing sync pulse will cause the rundown current to be increased several fold and speed the recovery of the sync separator by bringing C65 positive again.

From the emitter of buffer Q65, the signal again splits two ways, one path goes through C68 and R196 and exits the module via pin 38 as separated sync which the Color Lock module uses as a timing signal. The second path from the emitter of Q65 is through C67 and attenuator R191, R195 to the retriggerable monostable comprising Q67 and Q68 and associated components. This monostable is designed to trigger on the leading edge of sync, the leading edge of an equalizing pulse, or the leading edge of a vertical serration. The normal timeout period of the monostable is approximately 7 microseconds. However, during a sync pulse of normal width, the time constant of C70 is fast enough to allow the trailing edge of sync to reset the monostable, leaving the output slightly positive with respect to ground for several microseconds following sync. This sets up current-steering differential pair Q69 and Q70 so Q69 is turned off and Q70 is turned on immediately following a sync pulse.

Immediately after either an equalizing pulse or the leading edge of a vertical serration Q69 remains on, and Q70 off. A back porch clamp pulse generated by Q71 is then steered by either diode D19 or D20. After sync pulses, the clamp pulse is steered through diode D19, buffered by Q73, and sent to the Output Module through pin 40. After equalizing pulses, and after the leading edge of vertical serrations, the clamp pulse is steered through diode D20, buffered by transistor Q74, and sent to the Output Module through pin 39.

Feedforward/Feedback Clamps (sheet 2 of schematic, D-E/6-8)

From sync separator Q62 and Q63, the separated sync output takes a second path (via TP20) to the sample and hold circuit composed of IC8 and associated components. Diode-connected transistor IC8D and resistor R116 provide the pulldown load for the sync separator, Q62 and Q63. IC8C mirrors the current from the sync separator. During sync time, a 1 mA current is sent to differential pair IC8A and IC8B. The differential pair output is fed to mirror Q46 and Q47. The output of the circuit then goes to an integrating hold circuit composed of C51, C50, and R117. It is buffered by Q48 and Q49 and sent back to the base of IC8B. The video input to the sampler at pin 4 of the IC is an output of IC6, filtered and delayed by DL1B, which is a seven-pole Bessel filter providing flat group delay response to the sync signal. Since only the leading edge of sync has been delayed at IC8, pin 6, and the entire signal has been delayed at IC8, pin 4, the sample will occur only on the flat tip of sync and not during rising or falling edges. This minimizes clamping distortion.

The output of the sample and hold circuit is sent to three destinations. The first destination is through R105 to the integrator formed by IC13D and C42 (via TP4, 5 and 6) back to the input of the video input stage. This provides a feedback clamping function to null low frequency hum at the input node of the processor. The second path is through low pass filter R246 and C45 to amplifier IC5, through clamp adjust pots R131 and R133, to the two nodes of the remote gain amplifier (sheet 1, C/7). R131 and R133 are adjusted to null the feedforward clamping voltage at the two extremes of gain setting. The third path from the sample and hold circuit is through R114 and R145 to combining amplifier IC7 of sync separator 2.

Sync Separator 2 (sheet 2 of schematic, C/2-6)

Introduction

This separator provides sync for the external reference board and the sync generator board. Comp sync is also separated into vertical interval (9H) pulses and horizontal line pulses (9H-, = not 9H) which are used for clamping in the luminance amp of the output board (see Figure 6). Because of delays these pulses actually clamp during the back porch, after burst.

Description

The second input to IC7 is the output from IC6 through 1 microsecond delay line DL2, and its adjustable termination. R150 is adjusted to exactly null hum signals at the output of IC7. Due to the fact that the video into combining amplifier IC7 is delayed more than the sample from the sampling circuit, the actual clamping action begins during front porch time. This ensures that the leading edge of sync at the output of IC7 will be stable, independent of high or low frequency hum on the incoming signal.

The output of IC7 goes two places: first to the sync separating com parator, IC10, and second to the blanking level seeking circuit com posed of IC9 and associated components. By choosing the values of R162 and R163 (at IC9), the resulting charge on C59 will average through IC13C and D25 at blanking level. (Since the signal into the circuit has been solidly sync tip clamped to ground, this circuit effectively measures the average amplitude of sync.) (This circuit is a high gain comparator with a 16% mirror circuit determined by R162 and R163. Since the duty cycle of sync is approximately 8.5%, and the duty cycle of blanking is 23%, the 16% current mirror configuration in a closed loop causes this circuit to settle on the nominal blanking level of a signal.) The output measurement then goes to several destinations.

The first is to sync separator IC10 through the divider formed by R167 and R168. This precision divider assures that IC10 separates sync at the 50% point independent of the amplitude of sync over a 20 dB dynamic range. The second destination for the Automatic Tracking Control (ATC) voltage out of the blanking seeker is through the divider formed by R188 and R189 to the first sync separator. The third destination of the ATC voltage is through R172 to the clamp rundown circuit. This feedback path causes the rundown current on the signal fed to C65 to be a constant percentage of sync amplitude, ensuring a constant clamping action in the first clamp independent of the amplitude of sync over a wide dynamic range. The final destination for the ATC voltage is through R174 to amplifier IC13A. This amplifier's output is applied to IC6, to offset the output of IC6. The net effect, due to the overall behavior of the clamping circuit, is to offset the main video path of the processor in such a fashion that the processor is always operating in the center of its dynamic range.

Local Controls (sheet 2 of schematic, C-E/1-3)

The two sections of IC14 and associated components are ± 5 V regulators for the control circuitry of the processor. When the processor is in local mode, + and - 5 V are applied to both sides of the row of potentiometers R235 through R243. In the remote condition, the + and - 5 V are sent to the remote panel. If the LOCAL/REMOTE switch is in the remote position and CD and AB are strapped, both the local and the remote controls are active. This mode of operation is desirable in two cases: one, if only a single or possibly two remote controls are to be used, the local control potentiometers for those functions to be remoted would be set to the center of their range and all other controls would be local. The remote controls would be set with full range. The other case would be if several or all of the remote controls were used in a vernier fashion. A trim control range would be established by making the wiper arm resistor of the remote control panel on the order of 50K ohms. The local control would be used as a nominal setup point with the remote control centered, and the remote control then used as a vernier control.

Voltage Regulator

The regulator for the 3400/3200 Series modules receives ± 12 to 18 volts unregulated dc from the 3200A Power Supply and provides regulat ed ± 10 volts to the module. The incoming positive dc voltage is decoupled by L500 and C500. Further decoupling and current limiting is provided by C501 and RN501R. At startup, the regulator output is at zero, and series pass transistor Q502 is held off by RN501S. During startup, current flows through R500, RN501T, and R502, resulting in a small positive dc voltage at the output. This voltage is applied to the inverting input of IC500A through RN501K and RN501L. Network RN501N, R504, and RN501H divides this voltage in half and applies it to the non-inverting input of IC500A. The resulting input imbalance causes the output of IC500A to swing negative. The voltage developed across RN501P causes current to flow in Q503 and Q502. When Q502 is conducting, the output of the regulator rises until the voltage at the wiper arm of R504 is equal to the breakdown voltage of Q506 (6.45 V ± 4%). At this point, the IC inputs are balanced, and the loop stabilizes.

Operation of the negative regulator is similar to that of the positive regulator, except that IC500B is referenced to ground and connected to the output of the positive regulator. IC500B senses the difference between the positive and negative outputs through RN501D and RN501M. Thus, during normal operation, the negative regulator is tracking the positive regulator. However, if the negative output voltage is pulled toward ground due to the current limiting of Q501, the base of Q507 will be pulled positive. Q507 then goes into conduction, reducing the reference to the positive regulator. Thus, the positive regulator tracks the negative regulator during an overload condition.

The regulator comes in two versions. One is intended to supply less than 100 mA. This version has 4.7 ohm resistors for R500 and R501 and uses an MPSU51 transistor for Q502 and an MPSU01 for Q505. The second version supplies more than 100 mA. This version uses 2.7 ohm resistors for R500 and R501 and an MJE371 and MJE521 for Q502 and Q505 respectively.

ADJUSTMENTS

NOTE

The following adjustment procedure must be performed correctly before the Input Module is included in a system alignment.

Introduction

This procedure assumes that the Output Module, Color Lock Module, and the Sync Generator Module have been previously aligned.

Wide Band Oscilloscope	Tektronix 465
Wide Band Sweep Generator	Hewlett Packard 8601A
Digital Voltmeter	Weston 4440
TV Test Genertor (with 1 V p-p linearity ramp, color bars, and color black picture signals)	Tektronix 1411 (PAL) or 1410 (NTSC)

Refer to Component Location Drawing C07-066337-01.

Preliminary Conditions

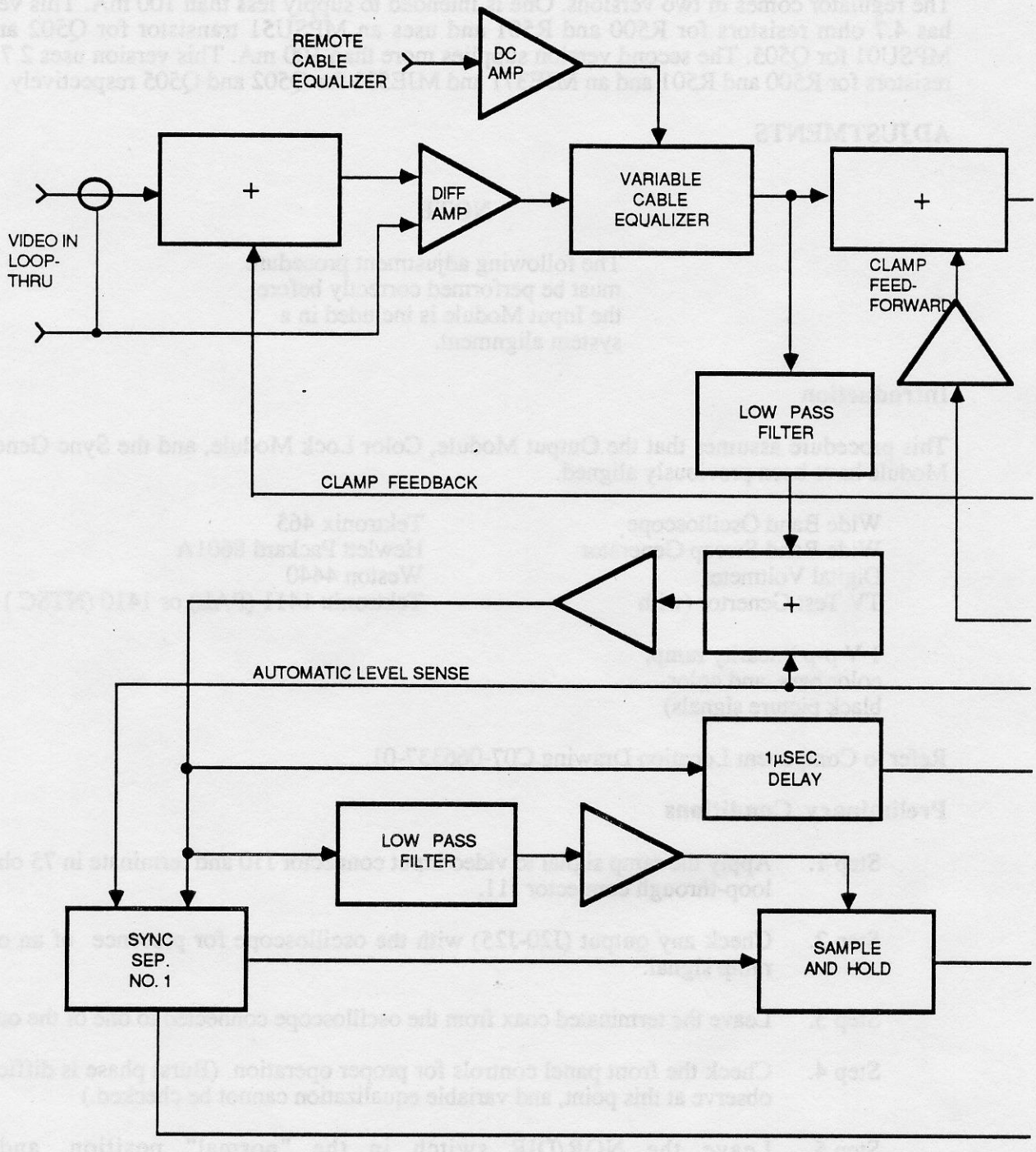
Step 1. Apply the ramp signal to video input connector J10 and terminate in 75 ohms at loop-through connector J11.

Step 2. Check any output (J20-J25) with the oscilloscope for presence of an output ramp signal.

Step 3. Leave the terminated coax from the oscilloscope connected to one of the outputs.

Step 4. Check the front panel controls for proper operation. (Burst phase is difficult to observe at this point, and variable equalization cannot be checked.)

Step 5. Leave the NOR/DIR switch in the "normal" position, and the LOCAL/REMOTE switch in the "local" position. Center all the front panel controls except the soft clip and hard clip, which should be set fully clockwise.


REMOTE CABLE EQUALIZER
DC AMP
VIDEO IN LOOP-THRU
+
DIFF AMP
VARIABLE CABLE EQUALIZER
+
CLAMP FEED-FORWARD
LOW PASS FILTER
CLAMP FEEDBACK
+
AUTOMATIC LEVEL SENSE
1μSEC. DELAY
LOW PASS FILTER
SYNC SEP. NO. 1
SAMPLE AND HOLD

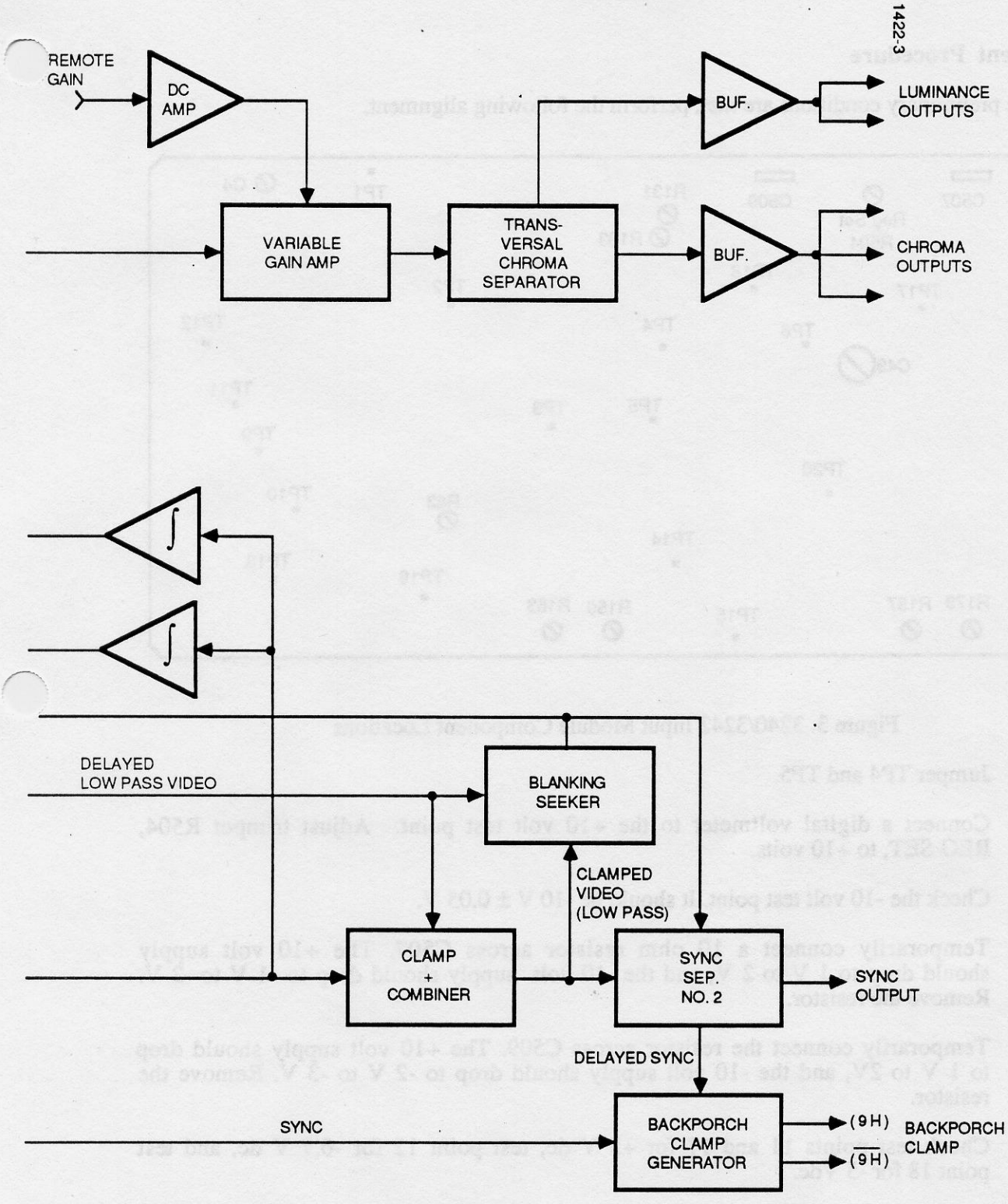


Figure 2. NTSC/PAL-M Input Module, Block Diagram

Alignment Procedure

After the preliminary conditions are met, perform the following alignment.

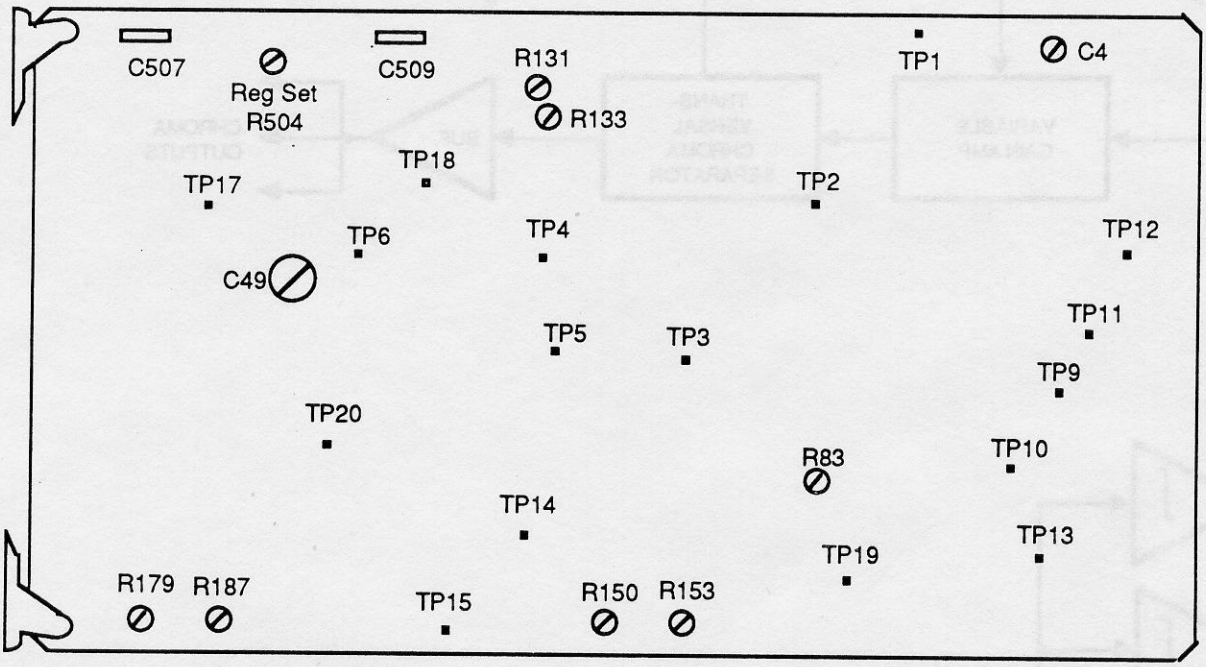


Figure 3. 3240/3242 Input Module Component Locations

Step 1. Jumper TP4 and TP5.

Step 2. Connect a digital voltmeter to the +10 volt test point. Adjust trimpot R504, REG SET, to +10 volts.

Step 3. Check the -10 volt test point. It should be -10 V ± 0.05 V.

Step 4. Temporarily connect a 10 ohm resistor across C507. The +10 volt supply should drop to 1 V to 2 V, and the -10 volt supply should drop to -1 V to -2 V. Remove the resistor.

Step 5. Temporarily connect the resistor across C509. The +10 volt supply should drop to 1 V to 2V, and the -10 volt supply should drop to -2 V to -3 V. Remove the resistor.

Step 6. Check test points 11 and 17 for +5 V dc, test point 12 for -0.7 V dc, and test point 18 for -5 Vdc.

Step 7. Apply the ramp signal to the input and monitor test point 1 with the oscilloscope. Check for an inverted ramp at 0.64 volt p-p.

Step 8. Monitor test point 2 with the oscilloscope. Check for a non-inverted ramp at approximately 1 V p-p.

Step 9. Monitor test point 20 with the oscilloscope. Remove the input signal. Turn potentiometer R179 fully clockwise, then back off until the signal just snaps from -10 to -7. Restore the input signal.

Step 10. Connect the test equipment as shown in Figure 2.

Step 11. Monitor test point 19 with the oscilloscope and adjust R150 for minimum hum on the sync tip.

Step 12. Monitor test point 3 with the oscilloscope. Set the video gain at maximum and adjust R131 for minimum. Set the video gain at minimum and adjust R133 for minimum hum. Repeat the procedure for balance.

Step 13. Monitor test point 6 with the oscilloscope and adjust C49 for a minimum axis shift during the sample. If sag between samples is greater than 12 mV p-p, replace Q48.

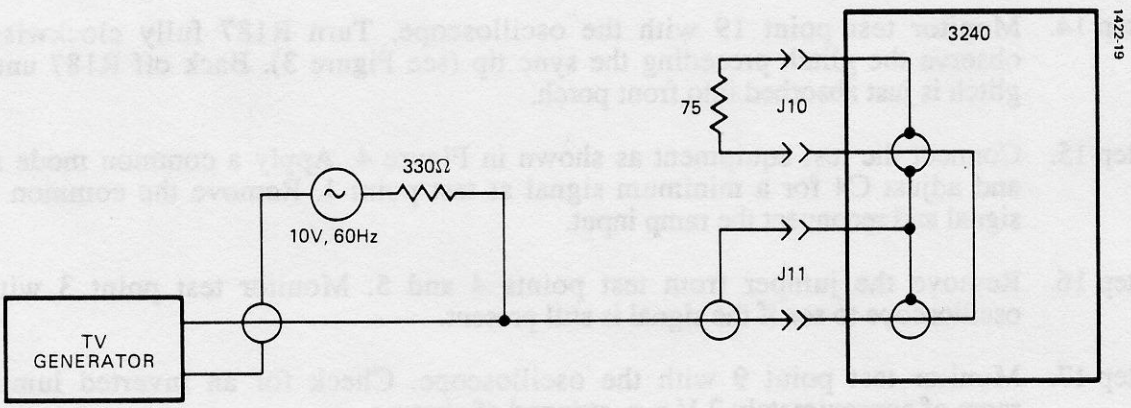


Figure 3. Differential Mode Hum Test Setup

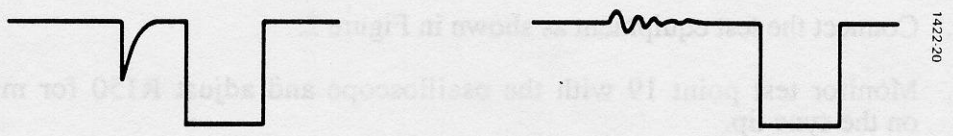


Figure 4. Sync Waveform

Step 14. Monitor test point 19 with the oscilloscope. Turn R187 fully clockwise and observe the glitch preceding the sync tip (see Figure 3). Back off R187 until the glitch is just absorbed into front porch.

Step 15. Connect the test equipment as shown in Figure 4. Apply a common mode signal and adjust C4 for a minimum signal at test point 1. Remove the common mode signal and reconnect the ramp input.

Step 16. Remove the jumper from test points 4 and 5. Monitor test point 3 with the oscilloscope to see if the signal is still present.

Step 17. Monitor test point 9 with the oscilloscope. Check for an inverted luminance ramp of approximately 2 V p-p, stripped of chroma.

Step 18. Monitor test point 10 with the oscilloscope. Check for a chroma signal of approximately 0.8 V p-p. Adjust R83 for a flat center line.

Step 19. Monitor test point 13 with the oscilloscope. Observe the leading edge of sync. Trigger on the input signal. Remove the termination and insert 6 dB of attenuation in the line. Adjust R153 for minimum delay change in the leading edge of sync when changing between 0 dB attenuation, 6 dB attenuation, and 12 dB attenuation (6 dB ± 6 dB).

Step 20. Set the oscilloscope to 5 V/div. at 0.1 ms/div., vertical trigger. Monitor test point 14 with the oscilloscope and observe the clamp pulse with the missing 9H (see Figure 5). The clamp pulses should be approximately 1 microsecond wide. Monitor test point 15 and observe the clamp pulse 9H only.

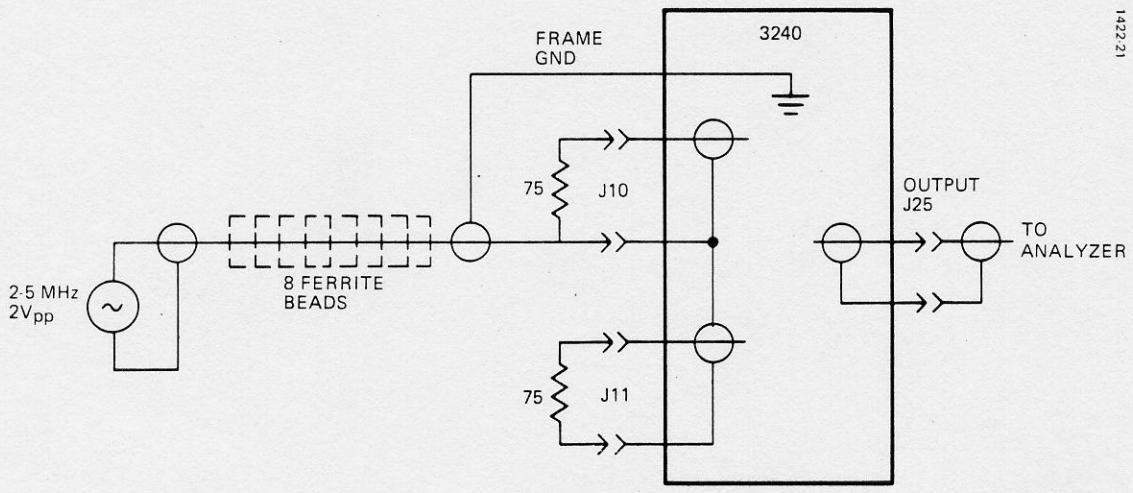


Figure 5. High Frequency Common Mode Test Setup

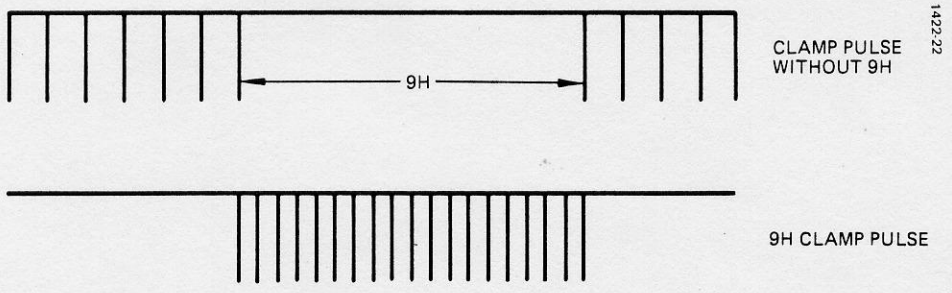


Figure 6. Clamp Pulse

INPUT AMPL

REMOTE GAIN AMPL

REMOTE CONTROL AMPLIFIERS

EQUALIZING AMPL

LUM AMPL

CHROMA AMPL

CHROMA SEPARATOR

POWER REGULATOR

REF. DWG - C10-058230-02

EQUALIZER BOARD ASSY. 063655-00

R1		CHG'D REV. STATUS	24NOV78
R2	9037	CORRECTED SCHEMATIC ERRORS PER ECO 9037	3FEB81
D1	9184	R46 WAS 1000.1%	27NOV84
D2	9283	Q15,Q16 CHANGED TO Q13,Q14	18MAR85
D3	9386	MOVED R60 & DEAPED TRACE	14JUL86
D4	9589	+10V OFF OF R1005 & R1008 WAS -10V	9-8-89
E1	9658	REG DWG # CHANGE	10-9-90
R1	9764	BOM CHANGE	27JUN96
FC	9821	R235-R240 WAS 1000Ω	6-11-96
H1	9932	ISSUE UPDATE	8-27-97
J1	99401	ISSUE UPDATE	8-27-97

UNLESS OTHERWISE SPECIFIED
ALL RESISTORS 1/4 W, 5%
ALL CAPACITORS ARE IN MICROFARADS
ALL DIODES ARE 1N4148
ALL NPN TRANSISTORS ARE MPS 6507
ALL PNP TRANSISTORS ARE MPS 6561
DENOTES CLOCKWISE ROTATION
LAST COMPONENT IDENT. NO. USED

MODULAR PRODUCTS | GRASS VALLEY GROUP

GTA	11MAY78	SCHEMATIC DIAGRAM 3240 PROCESSOR INPUT BOARD
LS	11MAY78	
3240	066337	E 10-066337-01

NONE

R1	1616	R160 WAS 4700Ω		
R2	1823	MOVED DES TO AGOS	STS	
R3	2553	D26 WAS D25, D25 ADDED TO ORIGINAL POSITION	STS	
D1	9184	G48 WAS MPS 6521, ADDED D27-IN4148	STS	
D2	9233	SEE SHEET 1	RRR	
D3	9306	SEE SHEET 1	EEE	

SAMPLE & HOLD

FEED BACK CLAMP INTEGRATOR

FEED FORWARD CLAMP AMPLIFIER

SYNC SEPARATOR 2

AUTOMATIC TRACKING CONTROL LINE

LOCAL CONTROLS

VIDEO GAIN	VIDEO GAIN
CHROMA GAIN	CHROMA GAIN
SET UP	SET UP
SYNC LEVEL	SYNC LEVEL
BURST LEVEL	BURST LEVEL
BURST PHASE	BURST PHASE
SOFT CLIP	SOFT CLIP
HARD CLIP	HARD CLIP
VAR EQ	VAR. EQ
LOCAL	-5V TO REMOTE PANEL
REMOTE	+5V TO REMOTE PANEL
NORMAL	NORMAL/DIRECT
DIRECT	

STRAP A-B & C-D FOR PARALLEL CONTROLS

J1-42	SYNC OUT
J1-40	CLAMP PULSE (EXCEPT 5H) TO OUTPUT BOARD
J1-39	CLAMP PULSE (5H ONLY) TO OUTPUT BOARD
J1-38	SYNC TO COLOR LOCK

PRODUCTS MODULAR

GRASS VALLEY GROUP

GTA 11MAY78 LS 11MAY78

SCHEMATIC DIAGRAM 3240 PROCESSOR INPUT BOARD

3240 066337

E:10-066337-01

NONE