NTSC COLOR LOCK MODULE

Manual Number: A90-066339-10 TP Number 06-077 Issue No.: 2

INTRODUCTION Refer to the block diagram of Figure 1.

The NTSC Color Lock Module uses a plug-in oscillator submodule which generates a frequency of 3.579545 MHz. The Color Lock Module regenerates the color burst signal (from the Input Module) by generating a color subcarrier reference signal and phase-locking the reference subcarrier to the incoming burst. The regenerated subcarrier is then routed to the Sync Generator Module, to the Output Module (only when used in 3240 Video Processing Amplifiers), and to the SUBCARRIER output connectors on the frame assembly.

Specific functions performed by the Color Lock Module are listed below and dicussed in the circuit description.

Subcarrier phase locking to incoming burst
Burst presence detection
Subcarrier output amplification
Subcarrier reference oscillator for free-run mode
On-board voltage regulation

CIRCUIT OVERVIEW Refer to Figure 1 and schematic diagram E10-066339-10.

High-passed video from the Input Module is applied to the burst phase detector and the burst amplitude detector. These two detectors are keyed on during burst (and for about 0.5 microsecond before and after burst) by the wide burst gate generator. The burst phase detector compares the phase of subcarrier produced by the VCXO with the input burst. The burst phase-error voltage is then filtered and sampled with the burst phase sample and hold.

The phase error locks to the VCXO via a two-speed loop filter. The fast speed allows fast lockup time and the ability to follow rapid changes in subcarrier phase. The loop speed is controlled by the speed switch, which senses an out-of-lock condition.

The VCXO has two subcarrier output amplifiers. One is an emitter follower that buffers subcarrier to the burst phase detector. The other is the subcarrier output amplifier, which drives two BNC connectors at the rear of the processor.

The output of the keyed burst amplitude detector is coupled through a filter which has longer delay than the corresponding filter after the burst phase detector. The resulting burst envelope pulse is applied first to a peak detector and to a voltage comparator which picks off the pulse at its half-amplitude point. The pulse from the burst envelope pickoff is then shortened in the sample

pulse generator. The resulting sample pulse occurs during burst and tracks the position of burst relative to sync (because of the wide burst generator). This pulse enables the burst phase sample-and-hold current.

The burst-envelope pulse is also applied to the burst presence detector. If input burst is less than approximately -8 dB (from 286 mV peak-to- peak) the VCXO goes into free run mode.

The burst lock logic will appropriately switch subcarrier off and on and cause it to lock or free run depending upon the condition of its inputs. The logic table is shown in Table 1.

CIRCUIT DESCRIPTION

Burst Phase Detector

High-passed video from the Input Module is buffered by emitter- follower Q13, and applied to phase detector IC5. IC5 compares input burst phase with subcarrier phase from the VCXO through a 90-degree delay line. It is keyed on by the wide burst gate generator, so only burst phase is detected.

The relative phase of the two input frequencies is detected as a difference in voltage at output pins 6 and 12. In detecting burst phase, any difference in voltage at these pins constitutes an error voltage pulse, which passes through a balanced low-pass filter and is buffered by a pair of emitter followers in IC6.

Burst Phase Sample-and-Hold

The sample-and-hold function is provided by an operational transcon ductance amplifier, IC7. Its output is a current, the amplitude of which is a function of the amplifier bias current applied to pin 5 and the differential voltage at its input. When the current to pin 5 is zero and/or the input differential voltage is zero, there is no output current.

Q15 and Q16 are a unity-gain feedback pair, with very high input impedance and low output impedance. At the beginning of the sample period (determined by the sample pulse generator via TP9) the circuit which includes IC7 and feedback pair Q15 and Q16 is enabled. It is an operational amplifier with negative feedback provided by R63. Resistors R60 through R63 cause the "op amp" to perform a balanced-to- single-ended conversion by setting the inverting gain equal to the non-inverting gain. When the sample period ends, IC7 turns completely off (via pin 5). The output of IC7 becomes a low-leakage open circuit to the "hold" capacitor, C31.

When the burst lock inhibit line (TP8) is high (0 volts), IC8 will clamp the burst phase sample-and-hold capacitor to ground by applying feedback to IC8 pin 2, which is forced to be equal to pin 3 by IC8.

Loop Filter and Speed Switch

The circuit which includes IC9 is an active two-speed loop filter. The time constants are altered by Q17 in such a manner that when it is turned on, the phase locked loop will acquire lock rapidly and follow rapid changes in phase.

The loop filter speed is changed automatically by sensing an out-of-phase condition at the output of the sample-and-hold. Under normal (locked or freerun) conditions, the output of the sample-and- hold will be zero volts. If there is a step of phase (during a nonsynchronous

switch), there will be an impulse of voltage at TP2. This is amplified by IC10(A) and full-wave rectified by IC10(B), D9, and D10. If the step of phase exceeds approximately 20 degrees, the negative peak impulse of voltage at IC10, pin 10, will exceed the negative voltage set at pin 9. The output at pin 8 will then charge C37 negative, which makes pin 14 positive and turns Q17 on (by turning D7 off). The loop filter will remain in fast mode for the period determined by C37 and R90.

Subcarrier Output Amplifier and Buffer

The output amplifier is a video amplifier with Q20 and Q21 functioning as a feedback pair and Q22 and Q23 as class B output drivers. R99 is the feedback resistor. The range of the subcarrier level pot is sufficient to achieve a one- or two-volt level of output subcarrier terminated in 75 ohms. Q24 is an emitter-follower to buffer the VCXO from the interboard wiring.

Burst Amplitude Detector and Sample Pulse Generator

IC1 is a balanced demodulator which is connected as a burst amplitude detector. The wide burst gate generator keys the detector on during back porch so that only burst amplitude is detected. The amplitude of burst is detected as a difference in current between pins 6 and 12. Zero amplitude causes zero difference in current. The current output is sensed as a differential voltage between resistor R4 and R5. The resulting burst envelope pulse passes through a balanced low-pass filter and is buffered by Q1 and Q2. IC3, R14-17 does the balanced-to-single-ended conversion and level-shifts the pulse to ground. D1 peak detects the pulse and stores it on C13. The output of Q3 is the peak amplitude voltage. R19 and R21 divide it in half and apply it to pin 5 of voltage comparator IC4(A). IC4(A) picks off the amplitude of the pulse at the 50% point. The output of IC4(A) is a negative-going pulse which is buffered by Q6. The duration of the pulse is shortened and inverted by Q12. The length is determined by C16 and R34. Table 1 lists the relationships between burst present and video present signals to output information.

Burst Presence Detector

The burst presence detector circuit provides a means of sensing a minimum of -8 dB of burst at the input of the processor and providing a logic output based on that information. IC4(B) compares the amplitude of output pulses from IC3 with a +.7 V reference developed by voltage divider R24, R25. Any portion of an incoming pulse that is greater in amplitude than +.7 V will appear as an output pulse from IC4. These pulses charge C55 through D14 to approximately +1.5 V. This voltage at the base of Q28 keeps it biased off. If input pulses to IC4 are absent or below +.7 V, the IC4 output will stop charging C55, and it will discharge through R123. This will bias the base of Q28 negative and it will conduct, causing the collector of Q27 to go from approximately +.7 V to -10 V (TP7). R28 provides hysteresis. C56 is a speed-up capacitor.

Burst Lock Logic

Q7, Q9, and Q10 form a three-input NAND gate. The threshold at which the NAND operates is determined by the voltage at the base of Q11. It is set at +.9 V by voltage divider R37, R42. A voltage more negative than +.9 V at any of the NAND transistor bases will cause their collectors, which are tied together, to go from -10 V to ground. This output is applied to Q18, IC8, and Q14, all of which act to switch the VCXO into a free-running state when they are at ground. When this output is at -10, the VCXO will be locked to the incoming burst. Q10 accepts input from the subcarrier lock enable line, the input to Q9 is video presence from the Sync Generator Module, and Q7 is driven by the burst presence output from Q27.

Q4 provides buffering for the burst flag inhibit output and the subcarrier inhibit line going to the VCXO. The base of Q4 is controlled by both burst presence information from Q5 and video presence information from Q29 through isolating diode D2.

TABLE 1. COLOR LOCK STATUS

Input Conditions		Output Status	
Burst Present?	Video Present	Subcarrier Locked to Burst?	Regenerated Burst?
No	No	No	Yes
No	Yes	No	No
Yes	No	No+	Yes+
Yes	Yes	Yes	Yes

+Noncomposite video is interpreted as "no input".

In the external reference mode the burst phase detector, burst phase sample and hold, and the loop filter are all disabled. The subcarrier error voltage developed by these circuits is replaced by an error voltage from the External Reference Module. This voltage is applied to the error input of the VCXO from pin 28 through R78. VIDEO PRESENCE and the burst presence detector retain control of the subcarrier inhibit and burst flag inhibit lines when in the external reference mode.

± 10 Volt Regulator Refer to schematic diagram C10-058030.

The ± 10 volt regulator receives ± 12 to 18 volts unregulated dc from the 3200A Power Supply and provides regulated ± 10 volts to the module. The incoming positive dc voltage is decoupled by L500 and C500. Further decoupling and current limiting is provided by C501 and RN501R. At startup the regulator output is at zero, and series-pass transistor Q502 is held off by RN501S. During startup, current flow through R500, RN501T, and R502, results in a small positive dc voltage at the output. This voltage is applied to the inverting input of IC500A through RN501K and RN501L. Network RN501N, R504, and RN501H divides this voltage in half and applies it to the noninverting input of IC500A. The resulting input imbalance causes the output of IC500A to swing negative and inject current through RN501P and Q503 to Q502. With Q502 conducting, the output of the regulator rises until the voltage at the wiper arm of R504 is equal to the breakdown voltage of Q506 (6.45 V ± 4%). At this point the IC inputs are balanced, and the loop stabilizes.

Operation of the negative regulator is similar to that of the positive regulator, except that IC500B is referenced to ground. Operational Amplifier IC500B senses the difference between the regulated positive and negative outputs through RN501D and RN501M, and adjusts the negative output to eliminate the difference. Thus, during normal operation, the negative regulator tracks the positive regulator output. If a current overload causes the negative output to be pulled toward ground Q507 will be pulled positive, and Q507 will conduct. With Q507 conducting, the reference to the positive regulator will be reduced, leading to a lowered output from the positive regulator. In this way, the positive regulator tracks the negative regulator output during overload conditions.

± 5 Volt Power Supply

The ± 5 V power supply is two IC op amp voltage followers which provide buffering for resistive dividers. The positive side consists of IC2(B) and divider pair R7 and R8. The negative side consists of IC2(A) and divider pair R9 and R10. C7, C8, C9, and C10 provide input and output filtering.

SERVICE NOTES

Subcarrier Oscillator

The oscillator plug-in assembly is not field repairable due to temperature compensation of the crystal. Oscillators must be returned to the factory for repair and realignment.

ADJUSTMENTS

NOTE
Adjustments have been made at the factory. Do not reset adjustments unless parts which affect the adjustments have been replaced.

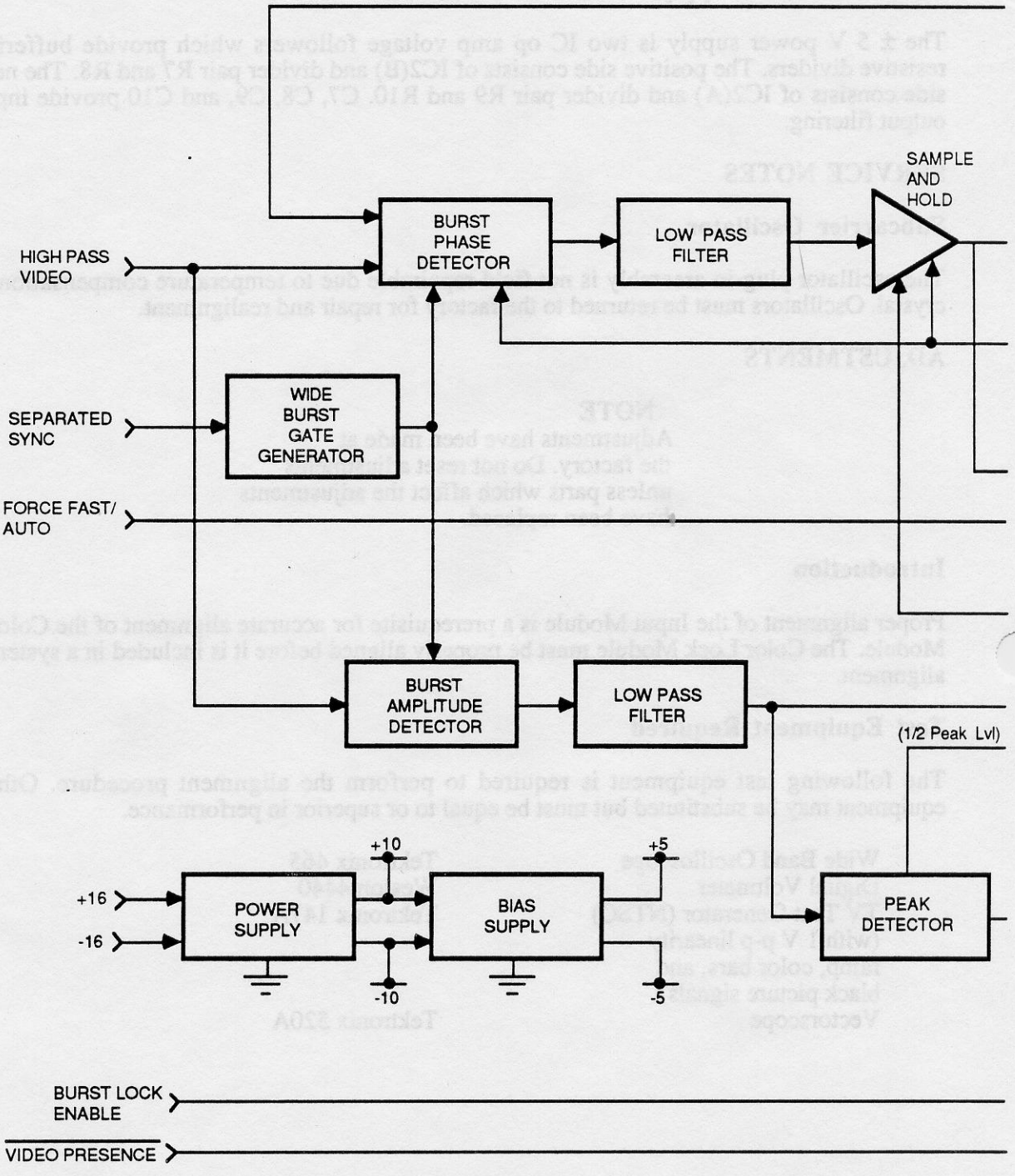
Introduction

Proper alignment of the Input Module is a prerequisite for accurate alignment of the Color Lock Module. The Color Lock Module must be properly aligned before it is included in a system-level alignment.

Test Equipment Required

The following test equipment is required to perform the alignment procedure. Other test equipment may be substituted but must be equal to or superior in performance.

Wide Band Oscilloscope	Tektronix 465
Digital Voltmeter	Weston 4440
TV Test Generator (NTSC) (with 1 V p-p linearity ramp, color bars, and black picture signals)	Tektronix 147A
Vectorscope	Tektronix 520A


SAMPLE
AND
HOLD
BURST
PHASE
DETECTOR
LOW PASS
FILTER
HIGH PASS
VIDEO
WIDE
BURST
GATE
GENERATOR
SEPARATED
SYNC
FORCE FAST/
AUTO
BURST
AMPLITUDE
DETECTOR
LOW PASS
FILTER
(1/2 Peak Lvl)
+10
+5
+16
-16
POWER
SUPPLY
BIAS
SUPPLY
PEAK
DETECTOR
-10
-5
BURST LOCK
ENABLE
VIDEO PRESENCE

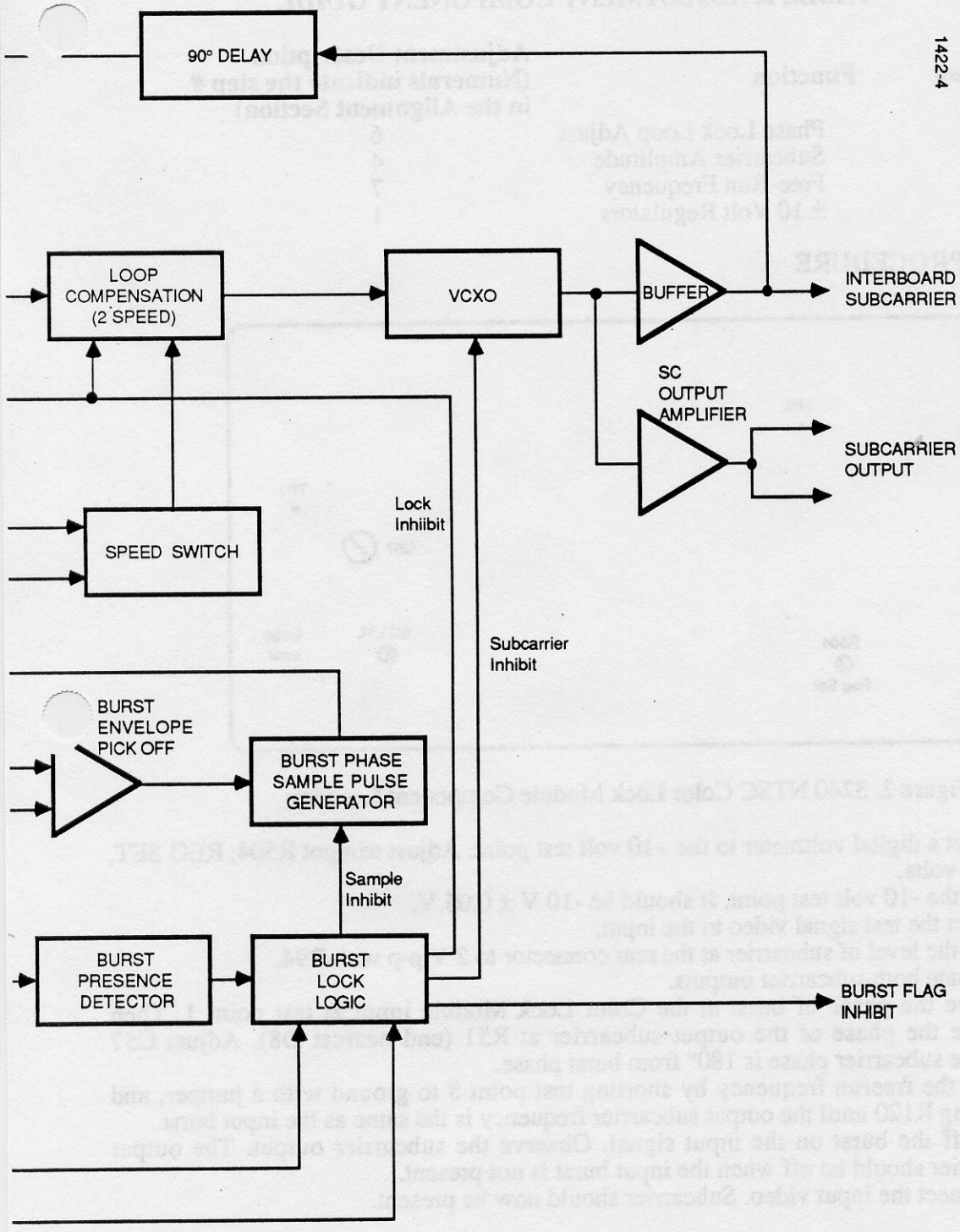


Figure 1. Functional Diagram, NTSC Color Lock Module

TABLE 2. ADJUSTMENT COMPONENT GUIDE

Component	Function	Adjustment Description (Numerals indicate the step # in the Alignment Section)
C57	Phase Lock Loop Adjust	6
R94	Subcarrier Amplitude	4
R120	Free-Run Frequency	7
R504	± 10 Volt Regulators	1

ALIGNMENT PROCEDURE

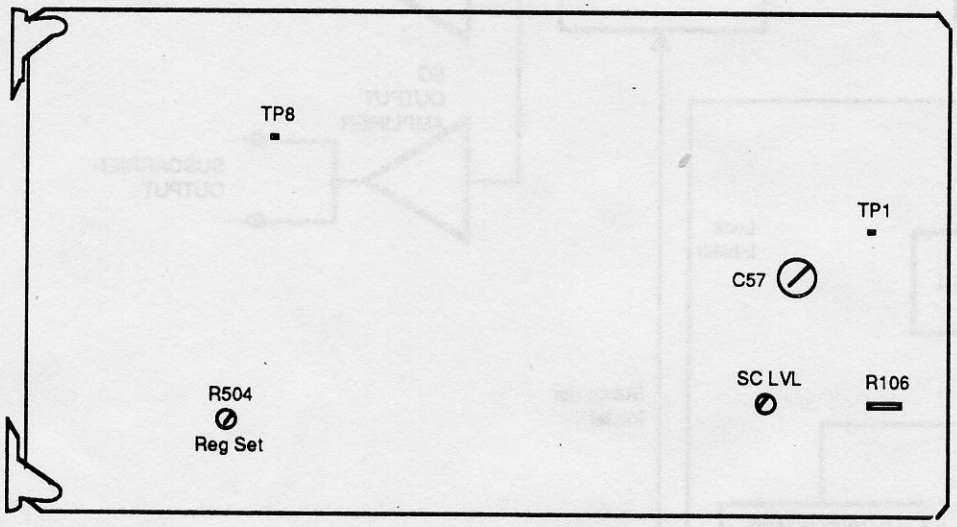


Figure 2. 3240 NTSC Color Lock Module Component Location

Step 1. Connect a digital voltmeter to the +10 volt test point. Adjust trimpot R504, REG SET, to +10 volts.

Step 2. Check the -10 volt test point. It should be -10 V ± 0.05 V.

Step 3. Connect the test signal video to the input.

Step 4. Adjust the level of subcarrier at the rear connector to 2 V p-p with R94.

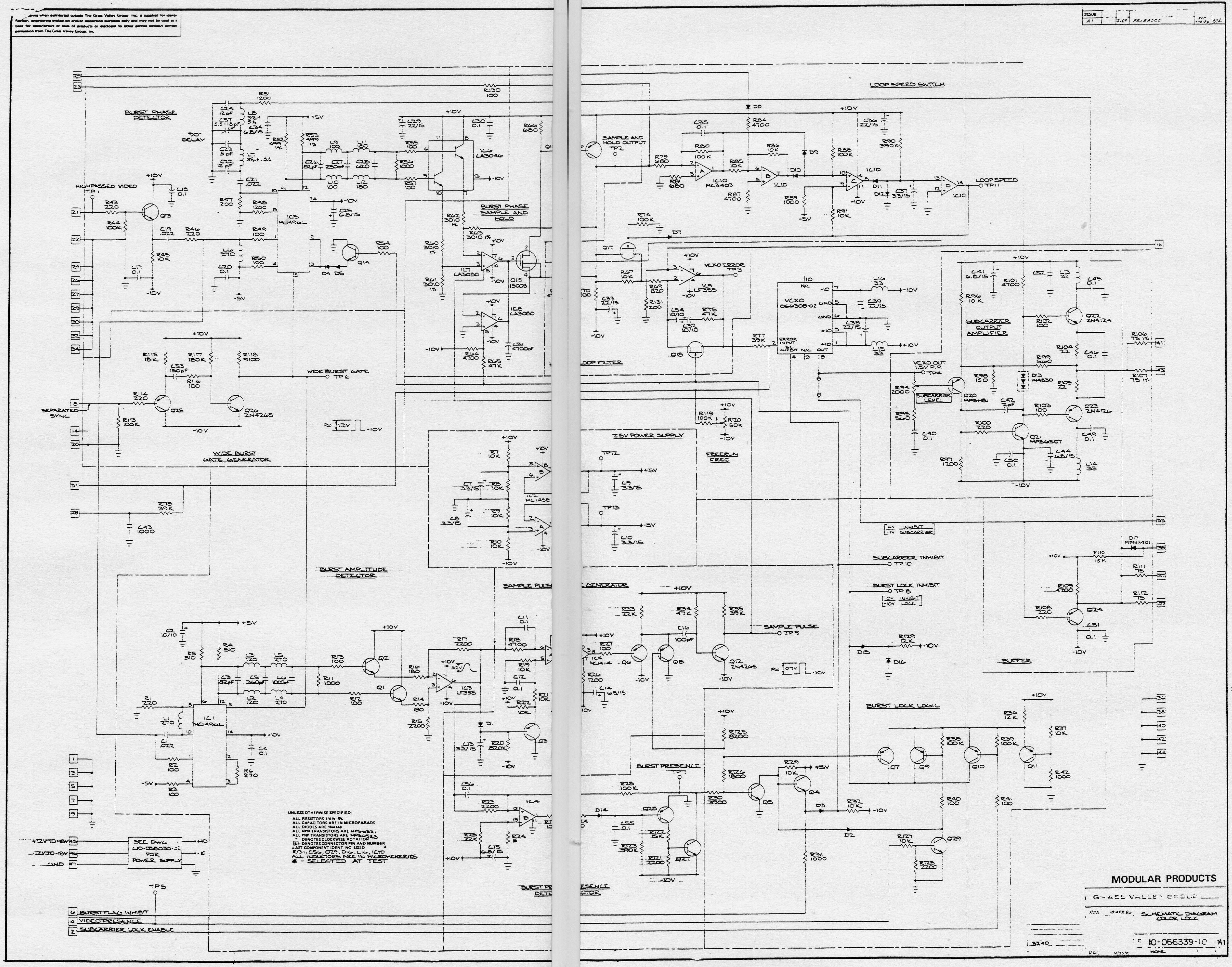
Step 5. Terminate both subcarrier outputs.

Step 6. Observe the phase of burst at the Color Lock Module input at test point 1. Then observe the phase of the output subcarrier at R51 (end nearest D8). Adjust C57 until the subcarrier phase is 180° from burst phase.

Step 7. Adjust the freerun frequency by shorting test point 8 to ground with a jumper, and adjusting R120 until the output subcarrier frequency is the same as the input burst.

Step 8. Turn off the burst on the input signal. Observe the subcarrier output. The output subcarrier should be off when the input burst is not present.

Step 9. Disconnect the input video. Subcarrier should now be present.



LOOP SPEED SWITCH
BURST PHASE DETECTOR
90° DELAY
HIGHPASSED VIDEO TP1
BURST PHASE SAMPLE AND HOLD
SAMPLE AND HOLD OUTPUT TP2
LOOP SPEED TP11
VCXO ERROR TP3
VCXO 066308-02
LOOP FILTER
WIDE BURST GATE TP6
SEPARATED SYNC
WIDE BURST GATE GENERATOR
SUBCARRIER OUTPUT AMPLIFIER
VCXO OUT 1.5V P-P TP4
SUBCARRIER LEVEL
±5V POWER SUPPLY
FREERUN FREQ
SUBCARRIER INHIBIT TP10
BURST LOCK INHIBIT TP8
BUFFER
BURST AMPLITUDE DETECTOR
SAMPLE PULSE GENERATOR
SAMPLE PULSE TP9
BURST LOCK LOGIC
BURST PRESENCE TP7
BURST PRESENCE DETECTOR
SEE DWG 010-058030-02 FOR POWER SUPPLY
+12V TO +18V
-12V TO -18V
GND
TP5
BURSTFLAG INHIBIT
VIDEO PRESENCE
SUBCARRIER LOCK ENABLE
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS 1/4 W 5%
ALL CAPACITORS ARE IN MICROFARADS
ALL DIODES ARE 1N4148
ALL NPN TRANSISTORS ARE MPS6521
ALL PNP TRANSISTORS ARE MPS6523
SELECTED AT TEST
MODULAR PRODUCTS
GRASS VALLEY GROUP
SCHEMATIC DIAGRAM COLOR LOCK
10-066339-10